REMARKS

Claims 1-6 and 8-14, 16-24 and 26-30 remain pending in the present application. Claim 7 has been previously cancelled. Claims 1, 8, 16, 18, 26 and 28 have been amended.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 1-6 and 8-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,751,983 to Abramson et al. ("Abramson") in view of U.S. Patent No. 6,065,103 to Tran et al. ("Tran").

Claims 1, 8, 18 and 28 have been amended to further bring out a feature of embodiments of the present invention. In particular, these claims have been amended to bring out that the store address is stored in a first storage (e.g., a memory ordering buffer) and is stored in a second storage (e.g., a trailing store buffer) if the store address is de-allocated from the first storage due to completion of the store instruction. Thus, during disambiguation, the first storage can be checked first for the appropriate address when processing a load instruction and then the second storage can be checked. Accordingly, the load instruction may be retired if the appropriate address is found in the first or second storage.

Such features are neither shown nor suggested by the Abramson and Tran references. It is noted that the language of Col. 11, lines 1-11 of Tran is referring to the speculative store buffer 44 that holds results for speculative store operations. Whether the store instruction has been retired and what actions take place in the load/store buffer when the store instruction is retired is not discussed in this text. In this text, a match of addresses indicates a new value for a store instruction. A load/store unit 20 in Tran includes a load/store buffer to store memory operations corresponding to an instruction. The load/store unit also includes the speculative store buffer 44 that stores a speculative state of one or more memory locations. In other words, as described at

Col. 5, lines 37-52, the speculative store buffer stores an address for a memory location and a speculative state for that memory location. The speculative state is based on one or more store memory operations affecting a given memory location. Accordingly, when doing dependency checking for a load memory operation, an address lookup is performed in the speculative store buffer 44, and if there is a hit, then the speculative state of the memory location is forwarded. If there is a miss, then the data cache 14 is accessed for the non-speculative state of a memory operation. (Col. 5, lines 53-65). Tran does not teach or suggest the disambiguation of a subsequent load operation using a first storage (such as the load/store unit 20) and this speculative store buffer as recited in the claims. Applicants refer to Fig. 4 (of Tran), which describes the processing of a load instruction that is different from the claimed invention. Abramson does not describe a trailing store buffer. Because of the differences in operation between the Trans and Abramson devices, there is no suggestion in these references to simply replace the load/store unit 20 of Tran with the memory ordering buffer (MOB) of Abramson.

Since features of the claims are neither taught nor suggested by Abramson. Reconsideration and withdrawal of the rejection of claims 1-6, 8-14, 16-24, and 26-30 under 35 U.S.C. § 103(a) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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